DIGITAL-TO-ANALOG CONVERTING CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a digital-analog converting circuit (called D/A converting circuit, hereinafter), which may be incorporated in a semiconductor integrated circuit, having voltage-dividing resisters.

Fig. 4 is an explanatory diagram schematically showing a construction of a conventional D/A converting circuit 40. The D/A converting circuit 40 is a circuit with a 3-bit resolution. Essentially, in the D/A converting circuit 40, $2^3=8$ resisters R having equal resistant values are connected in series between a reference potential terminal Vref and a ground terminal GND. The reference potential terminal Vref supplies a reference potential. The ground potential supplies a ground potential. When a digital signal (code) is input to a decoder circuit (not shown), one of switches SW0 to SW7 is selected and is turned on under the control of the decoder circuit. One of levels of nodes N0 to N7 corresponding to the ON switch is output from an output terminal OUT through an amplifier AMP. Thus, the reference potential and the ground potential are equally divided into eight so as to convert the digital signal to a desired analog signal. A PMOS transistor PMOS is connected between the reference potential terminal and the resisters R. The PMOS transistor PMOS is a switch for inhibiting an operation of the

circuit and for shutting off current consumption in response to an enable signal ENB.

Generally, as shown in Fig. 5, the switches SW0 to SW7 are implemented by analog switches. Each of the analog switches is a combination of a P-channel type MOS transistor (called PMOS transistor, hereinafter) PMOS and an N-channel type MOS transistor (called, NMOS transistor, hereinafter) NMOS. By combining the PMOS transistor and the NMOS transistor, the ON resistances of the switches can be closer to a constant value. Figs. 6A to 6C are explanatory diagrams each showing a relationship between a potential to be applied to a MOS transistor and an ON resistance of the MOS transistor. Fig. 6A shows an ON resistance of the PMOS transistor. Fig. 6B shows an ON resistance of the NMOS transistor. Fig. 6C shows a composite resistance of the ON resistances of the PMOS transistor and NMOS transistor.

However, the conventional D/A converting circuit has problems regarding the conversion precision and the conversion speed.

As shown in Fig. 6C, the composite resistance of ON resistances of the analog switches is not completely constant and depends on the input side potential. In the conventional D/A converting circuit, the nodes N0 to N7 corresponding to the switches SW0 to SW7 have different potentials from each other. Thus, the composite resistances of the ON resistances of the

switches are not constant. As a result, the D/A conversion precision can be hardly improved.

Furthermore, as described above, the analog switches have the ON resistances. Due to the ON resistances and the parasitic capacitance within the circuit, the voltage level shifting in the output side takes time. Therefore, the conversion speed can be hardly improved.

SUMMARY OF THE INVENTION

The invention may provide a novel and improved D/A converting circuit, which can improve the conversion precision and conversion speed of digital-to-analog conversion.

According to an aspect of the invention, there is provided a digital-to-analog converting circuit includes first and second potential terminals, an output node, first and second resisters, first and second switches and control circuit. The first resisters are connected in series between a first node and the output node through first connecting points. Each of the first switches is connected between the first potential terminal and one of the first connecting points and the first node. The second resisters are connected in series between a second node and the output node through second connecting points. Each of the second switches is connected between the second potential terminal and one of the second connecting points and the second node. The control circuit controls the first and second

switches.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an explanatory diagram of a D/A converting circuit;

Fig. 2 is an explanatory diagram of a decoder circuit for controlling gates of MOS transistors in Fig. 1;

Fig. 3 is an explanatory diagram of another decoder circuit for controlling gates of the MOS transistors in Fig. 1;

Fig. 4 is an explanatory diagram of a conventional D/A converting circuit;

Fig. 5 is an explanatory diagram of an analog switch; and

Figs. 6A to 6C are explanatory diagrams of ON resistances; Fig. 6A shows an ON resistance of a PMOS transistor; Fig. 6B shows an ON resistance of an NMOS transistor; and Fig. 6C shows an ON resistance of an analog switch.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of a digital-to-analog converting circuit (D/A converting circuit) according to the invention will be described below in detail with reference to appended drawings. In this specification and the drawings, the same reference numerals are given to components having substantially the same functional constructions. The repeated description will be omitted.

This embodiment has switches between a reference potential and voltage-dividing resisters and between a ground potential and voltage-dividing resisters. Thus, a constant potential can be applied to switches. No analog switch is used as the switch.

Fig. 1 is a construction diagram schematically showing a D/A converting circuit according to this embodiment. In this embodiment, a D/A converting circuit 10 has a resolution of n=3. However, the invention can be applied to a resolution of any bit.

As shown in Fig. 1, the D/A converting circuit 10 includes a reference potential terminal Vref, a ground potential terminal GND, an amplifier AMP, an output terminal OUT, $(2^n-1)=7$ reference potential side resisters R1, $(2^n-1)=7$ PMOS transistors P1 to P7, $(2^n-1)=7$ ground potential side resistors R2, and $2^n=8$ NMOS transistors N0 to N7. The reference potential terminal Vref supplies a reference potential. The ground potential terminal GND supplies a ground potential. The amplifier AMP amplifies analog signals. The output terminal OUT outputs analog signals. The reference potential side resistors R1 are connected in series between the reference potential terminal Vref and the output terminal OUT. The PMOS transistors P1 to P7 correspond to the reference potential side resistors R1. The ground potential side resistors R2 are connected in series between the ground potential terminal GND and the output terminal OUT. The NMOS transistors N0 to N7 correspond to the ground potential side

resistors R2.

Sources of the reference potential side resistors R1 are connected to the reference potential terminal Vref. Drains of the reference potential side resistors R1 are connected to the output terminal OUT through the amplifier AMP. The gates of the reference potential side resistances R1 are connected to a decoder circuit 20, which will be described later. The reference potential side resisters R1 have equal resistance values.

The PMOS transistors P1 to P7 function as switches for switching paths can be selected between the reference potential terminal Vref and the reference potential side resistors R1 and for changing the number of the reference potential side resistors R1 from one to seven between the reference potential terminal Vref and the output terminal OUT. In other words, one of the PMOS transistors P1 to P7 is turned on so that one of the paths between the reference potential terminal Vref and the output terminal OUT. Thus, the number of the reference potential side resistors R1 between the reference potential terminal Vref and the output terminal OUT is changed from one to seven.

Ground Potential Side Resistors R2

Sources of the ground potential side resisters R2 are connected to the ground potential terminal GND. Drains of the ground potential side resistors R2 are connected to the output

terminal OUT through the amplifier AMP. The gates of the ground potential side resisters R2 are connected to the decoder circuit 20, which will be described later. The ground potential side resisters R2 have equal resistance values. The resistance values are equal to those of the reference potential side resisters R1.

The NMOS transistors N0 to N7 function as switches for switching paths between the ground potential terminal GND and the ground potential side resisters R2 and for changing the number of the ground potential side resistors R2 from zero to seven between the ground potential terminal GND and the output terminal OUT. In other words, one of the NMOS transistors N0 to N7 is turned on so that one of the paths can be selected between the ground potential terminal GND and the output terminal OUT. Thus, the number of the ground potential side resistors R2 between the ground potential terminal GND and the output terminal OUT is changed from one to seven.

Next, the switching control of the PMOS transistors P1 to P7 and NMOS transistors N0 to N7 will be described. Fig. 2 is an explanatory diagram of a decoder circuit for controlling the PMOS transistors P1 to P7 and the NMOS transistors N0 to N7.

As shown in Fig. 2, the decoder circuit 20 is a logical circuit including input terminals bit 0, bit 1 and bit 2. One bit digital signal is input to each of the input terminals bit

0, bit 1 and bit 2. The output terminal is connected to the gates of the PMOS transistor P1 to P7 and the gates of the NMOS transistors N0 to N7.

An inverse signal of an input signal from the input terminal bit2, an inverse signal of an input signal from the input terminal bit 1 and an inverse signal of an input signal from the input terminal bit 0 are input to a three-input AND gate A0. The output signal of the three-input AND gate A0 is input to a gate of the NMOS transistor N0 in Fig. 1.

An inverse signal of an input signal from the input terminal bit2, an inverse signal of an input signal from the input terminal bit 1 and an input signal from the input terminal bit 0 are input to a three-input AND gate A1. An output signal of the three-input AND gate A1 is input to a gate of the NMOS transistor N1 in Fig. 1. An inverse signal of an output signal is input to the PMOS transistor P1 in Fig. 1.

An inverse signal of an input signal from the input terminal bit2, an input signal from the input terminal bit 1 and an inverse signal of an input signal from the input terminal bit 0 are input to a three-input AND gate A2. An output signal of the three-input AND gate A2 is input to a gate of the NMOS transistor N2 in Fig. 1. An inverse signal of the output signal is input to the PMOS transistor P2 in Fig. 1.

An inverse signal of an input signal from the input terminal bit2, an input signal from the input terminal bit 1 and an input

signal from the input terminal bit 0 are input to a three-input AND gate A3. An output signal of the three-input AND gate A3 is input to a gate of the NMOS transistor N3 in Fig. 1. An inverse signal of the output signal is input to the PMOS transistor P3 in Fig. 1.

An input signal from the input terminal bit2, an inverse signal of an input signal from the input terminal bit 1 and an inverse signal of an input signal from the input terminal bit 0 are input to a three-input AND gate A4. An output signal of the three-input AND gate A4 is input to a gate of the NMOS transistor N4 in Fig. 1. An inverse signal of the output signal is input to the PMOS transistor P4 in Fig. 1.

An input signal from the input terminal bit2, an inverse signal of an input signal from the input terminal bit 1 and an input signal from the input terminal bit 0 are input to a three-input AND gate A5. An output signal of the three-input AND gate A5 is input to a gate of the NMOS transistor N5 in Fig. 1. An inverse signal of the output signal is input to the PMOS transistor P5 in Fig. 1.

An input signal from the input terminal bit2, an input signal from the input terminal bit 1 and an inverse signal of an input signal from the input terminal bit 0 are input to a three-input AND gate A6. An output signal of the three-input AND gate A6 is input to a gate of the NMOS transistor N6 in Fig. 1. An inverse signal of the output signal is input to the PMOS

transistor P6 in Fig. 1.

An input signal from the input terminal bit2, an input signal from the input terminal bit 1 and an input signal from the input terminal bit 0 are input to a three-input AND gate A7. An output signal of the three-input AND gate A7 is input to a gate of the NMOS transistor N7 in Fig. 1. An inverse signal of the output signal is input to the PMOS transistor P7 in Fig. 1.

When an enable signal EN is "0", the three-input AND gates A0 to A7 turn OFF all of the PMOS transistors P1 to P7 and NMOS transistors N0 to N7. Therefore, the operation of the D/A converting circuit 10 is inhibited, and the current consumption is shut off.

Three bit digital signals to be input to the decoder circuit 20 may be represented by (input value of the input terminal bit2, input value of the input terminal bit1, input value of the input terminal bit 0). When the three bit digital signals are (0,0,0), the NMOS transistor N0 is turned on in accordance with the output value of the three-input AND gate A0. The other transistors are turned off. Here, referring back to Fig. 1, the ground potential is output from the output terminal OUT.

Similarly, when the three bit digital signals are (0,0,1), the PMOS transistor P1 and the NMOS transistor N1 are turned on in accordance with the output value of the three-input AND gate A1. The other transistors are turned off. In this case,

the reference potential ×1/8 is output from the output terminal.

When the three bit digital signals are (0,1,0), the PMOS transistor P2 and the NMOS transistor N2 are turned on in accordance with the output value of the three-input AND gate A2. The other transistors are turned off. In this case, the reference potential ×2/8 is output from the output terminal.

When the three bit digital signals are (0,1,1), the PMOS transistor P3 and the NMOS transistor N3 are turned on in accordance with the output value of the three-input AND gate A3. The other transistors are turned off. In this case, the reference potential ×3/8 is output from the output terminal.

When the three bit digital signals are (1,0,0), the PMOS transistor P4 and the NMOS transistor N4 are turned on in accordance with the output value of the three-input AND gate A4. The other transistors are turned off. In this case, the reference potential ×4/8 is output from the output terminal.

When the three bit digital signals are (1,0,1), the PMOS transistor P5 and the NMOS transistor N5 are turned on in accordance with the output value of the three-input AND gate A5. The other transistors are turned off. In this case, the reference potential ×5/8 is output from the output terminal.

When the three bit digital signals are (1,1,0), the PMOS transistor P6 and the NMOS transistor N6 are turned on in accordance with the output value of the three-input AND gate A6. The other transistors are turned off. In this case, the

reference potential ×6/8 is output from the output terminal.

When the three bit digital signals are (1,1,1), the PMOS transistor P7 and the NMOS transistor N7 are turned on in accordance with the output value of the three-input AND gate A7. The other transistors are turned off. In this case, the reference potential ×7/8 is output from the output terminal.

As described above, according to this embodiment, the PMOS transistors P1 to P7 (reference potential side switches) are used for switching paths between the reference potential terminal Vref and the reference potential side resisters R1. Therefore, all of the potentials to be applied to the PMOS transistors P1 to P7 are the reference potential and are common. Thus, the composite resistances of ON resistances are all constant in the PMOS transistors. The same is true in the NMOS transistors N0 to N7 (ground potential side switches). As a result, the precision of the D/A conversion can be improved.

The PMOS transistors P1 to P7 and the NMOS transistors N0 to N7 are used as the switches. No analog switches are used. Thus, the delay of voltage level shifting due to parasitic capacitance within the circuit can be prevented. Therefore, the conversion speed can be improved.

Furthermore, this embodiment has following advantages.

The size of each of the voltage-dividing resistors does not affect on the entire size of the D/A converting circuit 10 significantly. Therefore, increases in the numbers of the

reference potential side resisters R1 and the ground potential side resisters R2 do not affect on the size of the D/A converting circuit 10 significantly.

A switch specifically for inhibiting circuit operations is not required. Therefore, an easy design is required for correcting precision errors due to ON resistances of the MOS transistors.

The decoder circuit 20 is a logical circuit. Therefore, the decoder circuit 20 is especially effective when the decoder circuit 20 is incorporated in a semiconductor integrated circuit.

All of the resisters in the circuit have an equal size. Therefore, this embodiment is suitable for a semiconductor integrated circuit, which may be different in accordance with the production.

According to a second embodiment, the construction of a decoder circuit is changed so as to be used as a D/A converting circuit having a low resolution.

Fig. 3 is an explanatory diagram schematically showing a decoder circuit in a D/A converting circuit according to this embodiment. The decoder circuit 20 shown in Fig. 2 is replaced by a decoder circuit 30. The rest of the construction is substantially the same as that of the first embodiment. Therefore, the repeated description will be omitted.

As shown in Fig. 3, the decoder circuit 30 is a logical circuit. The decoder circuit 30 includes input terminals bit0,

bit1 and bit2 to each of which one bit digital signal is input. An output terminal of the decoder circuit 30 is connected to gates of the PMOS transistors P1 to P7 and gates of the NMOS transistors N0 to N7. The decoder circuit 30 is different from the decoder circuit 20 in Fig. 2 in that a select signal SEL is added for selecting an operation.

When the select signal SEL is "1", "0" is input to one input terminal of two-input OR gates O1 to O6. Thus, substantially the same operation is performed as that of the first embodiment.

When the select signal SEL is "0", "1" is input to one input terminal of the two-input OR gate O1 to O4. Thus, the PMOS transistors P1 to P4 are always OFF. Also, "0" is input to one input terminal of the two-input AND gates A8 to A11. Thus, the NMOS transistors N4 to N7 are always OFF.

When the select signal SEL is "0", "1" is input to one input terminal of the two-input OR gates O5 and O6. Thus, the value of the input terminal bit2 does not affect on output values of the latter three-input AND gates A0 to A7. In other words, 2^2=4 types of level are selected based on the input values of the input terminals bit0 and bit 1, independently from the input value of the input terminal bit2.

Operations of Second Embodiment

Here, three bit digital signals to be input to the decoder circuit 30 are expressed by (-, input value of input terminal

bit1, input value of input terminal bit0) where the input value of the input terminal bit2 of three-bit digital signals is ignored. When the three-bit digital signals are (-, 0, 0), the NMOS transistor N0 is turned on in accordance with the output value of the three-input AND gate A0. The other transistors are turned off. In this case, referring back to Fig. 1, the ground potential is output from the output terminal OUT.

Similarly, when the three bit digital signals are (-,0,1), the NMOS transistor N1 and the PMOS transistor P5 are turned on in accordance with the output values of the three-input AND gates A1 and A5. The other transistors are turned off. In this case, the ground potential ×1/4 is output from the output terminal OUT.

When the three bit digital signals are (-,1,0), the NMOS transistor N2 and the PMOS transistor P6 are turned on in accordance with the output values of the three-input AND gates A2 and A6. The other transistors are turned off. In this case, the ground potential ×2/4 is output from the output terminal OUT.

When the three bit digital signals are (-,1,1), the NMOS transistor N3 and the PMOS transistor P7 are turned on in accordance with the output values of the three-input AND gates A3 and A7. The other transistors are turned off. In this case, the ground potential ×3/4 is output from the output terminal OUT.

As described above, according to this embodiment, in addition to the first embodiment, the D/A converting circuit 10 according to the first embodiment for a 3-bit resolution can be used for a two-bit resolution. When the same change is given to the input bit1 of the decoder circuit, the D/A converting circuit 10 can be used for a one-bit resolution. In other words, an arbitrary resolution can be selected and be used if the selected resolution is equal to or less than the maximum resolution inherent to the D/A converting circuit.

The preferred embodiments of the digital-to-analog converting circuit according to the invention have been described with reference to the appended drawings. However, the invention is not limited to those embodiments. Apparently, those skilled in the art can reach to various change examples and/or modification examples within the scope of the claimed technical principle. It is understood that the change examples and modification examples are apparently included in the technical scope of the invention.

For example, each of the embodiments includes a decoder circuit (20 or 30). All of the PMOS transistors P1 to P7 provided on the reference potential terminal Vref side and the NMOS transistors N0 to N7 provided on the ground potential terminal GND side are controlled by the single decoder circuit (20 or 30). However, the invention is not limited thereto. Alternatively, a first decoder circuit and a second decoder

circuit may be provided separately. The first decoder circuit controls the PMOS transistors P1 to P7 provided on the reference potential terminal Vref side. The second decoder circuit controls the NMOS transistors N0 to N7 provided on the ground potential terminal GND.